Abstract of the Disclosure

A programmable logic integrated circuit device has a plurality of areas of programmable logic disposed on the device in a two-dimensional array of intersecting rows and columns of such areas. A so-called "fast conductor" network is provided on the device for rapidly and efficiently distributing a relatively small number of signals to substantially any logic area on the device. The fast conductor network has several main conductors that substantially bisect the array in one direction (e.g., by extending parallel to the column axis). Some main conductors can carry signals from off the device. Other main conductors can carry signals generated on the device. The network further includes secondary conductors that extend transverse to the main conductors (e.g., along each row of logic areas). Programmable logic connectors are provided for selectively applying signals from the main conductors to the secondary conductors and from the secondary conductors to the logic areas.